

FIG .1

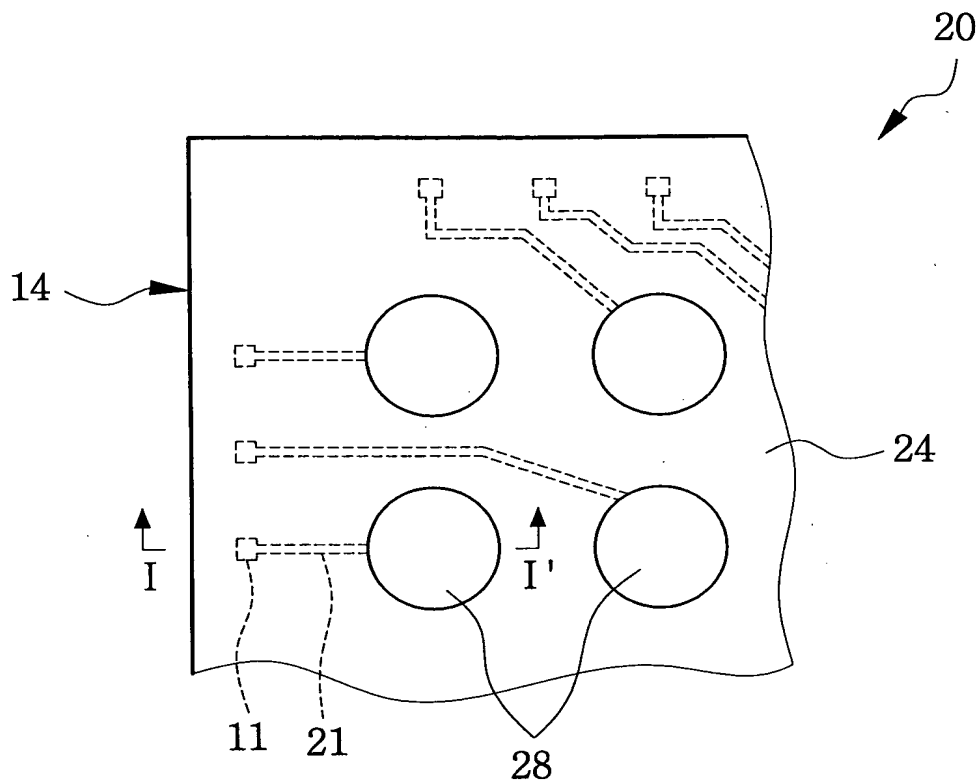
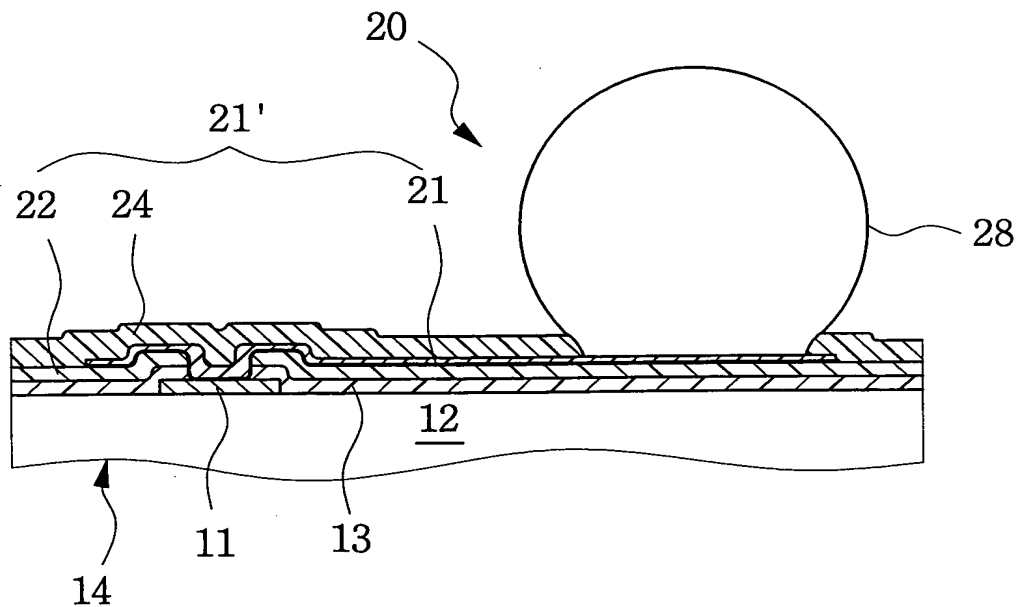


FIG .2



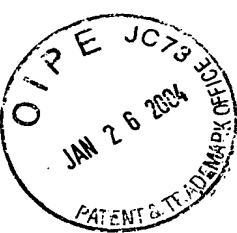


FIG .3

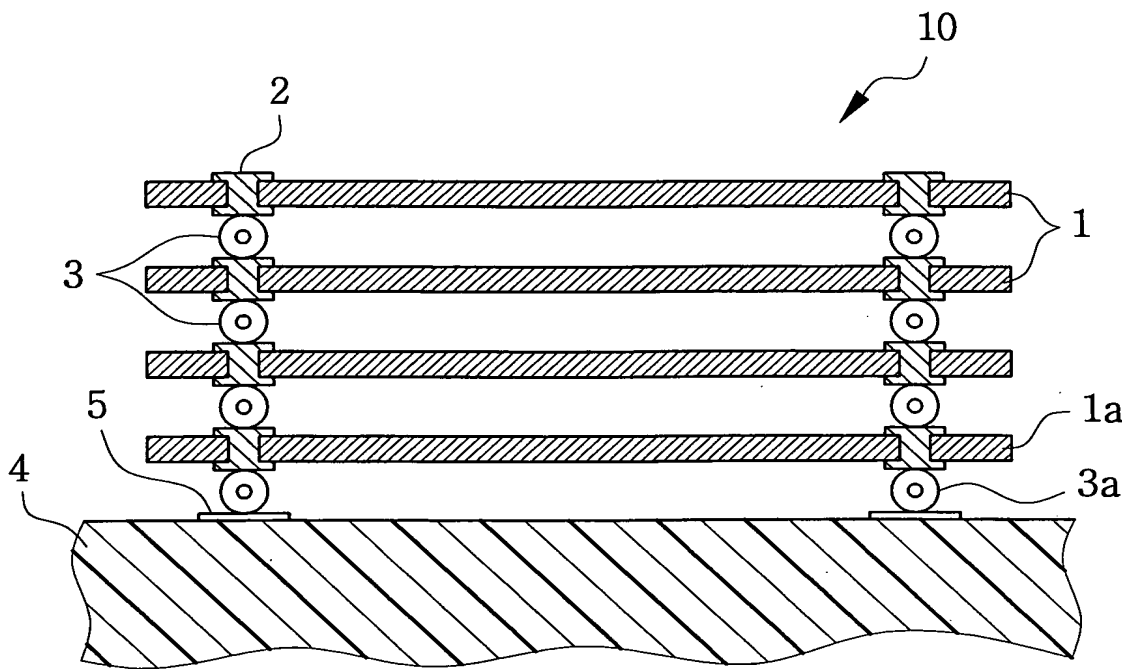
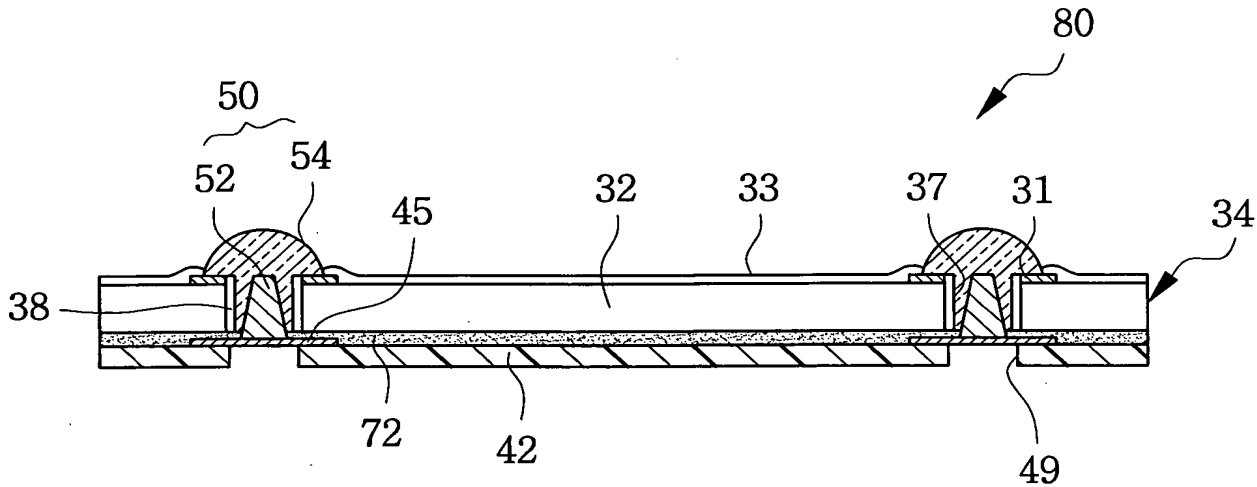


FIG .4



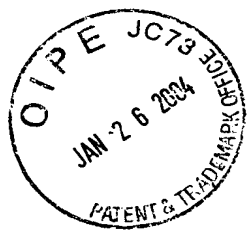


FIG .5

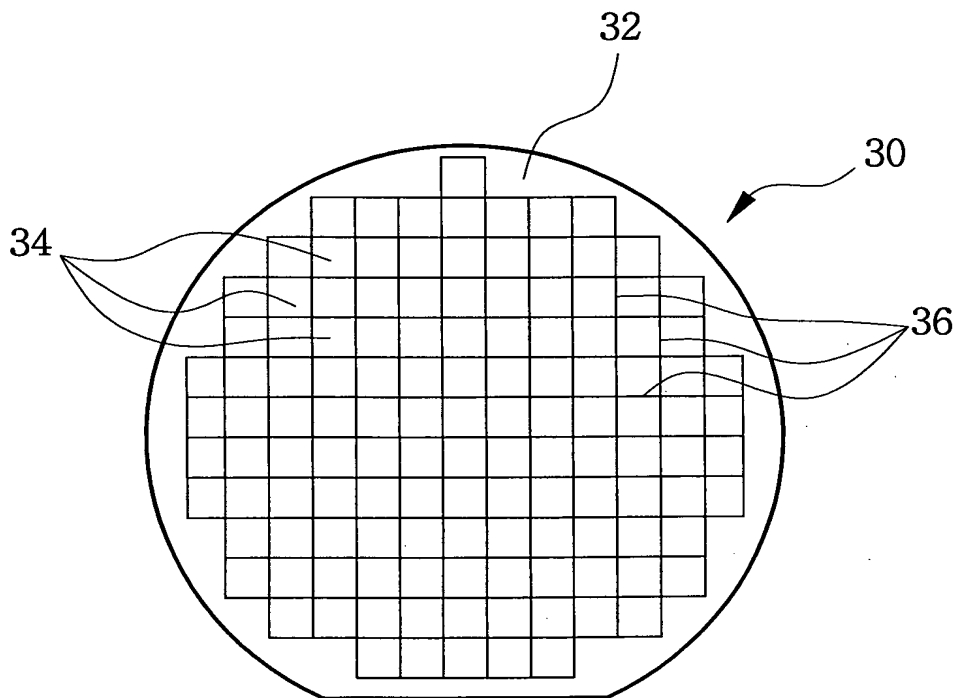
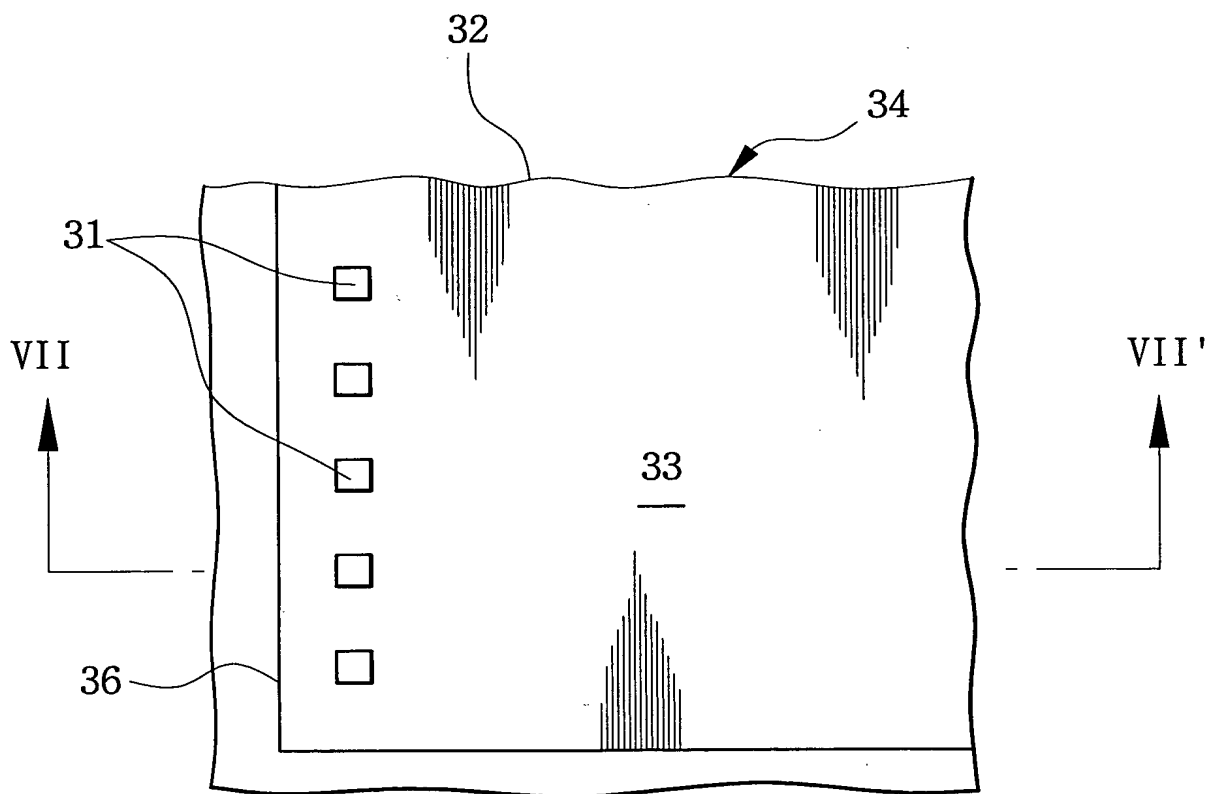
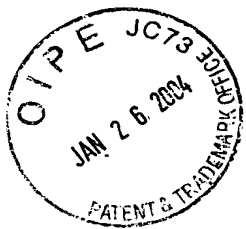


FIG .6





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FIG .7

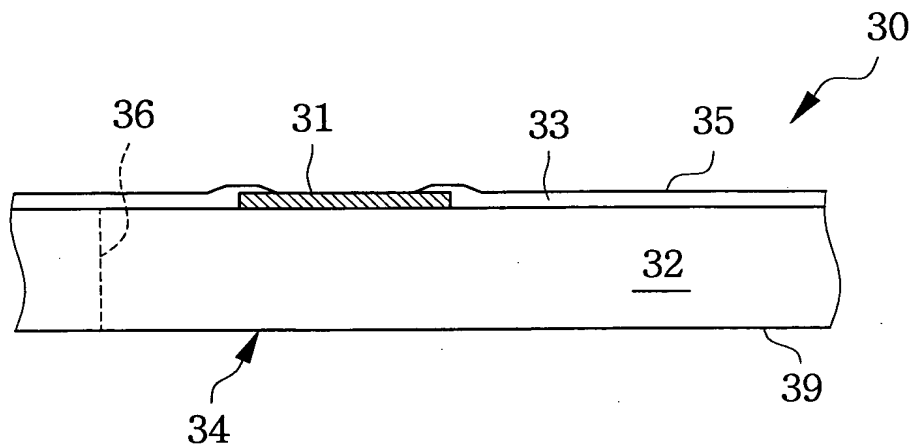
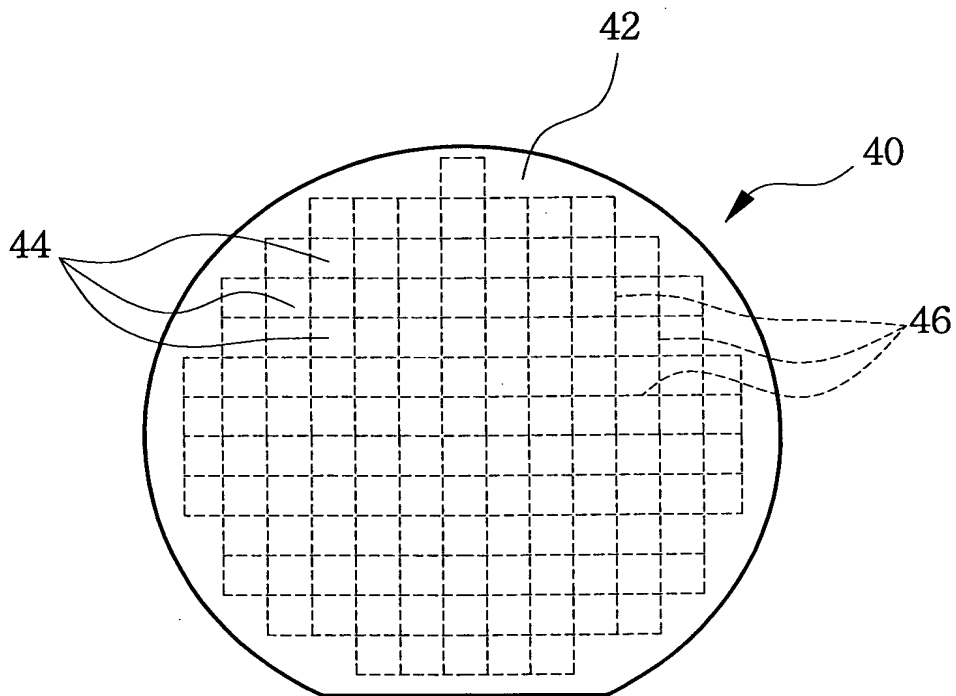


FIG .8



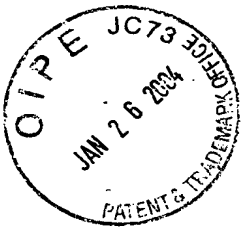


FIG .9

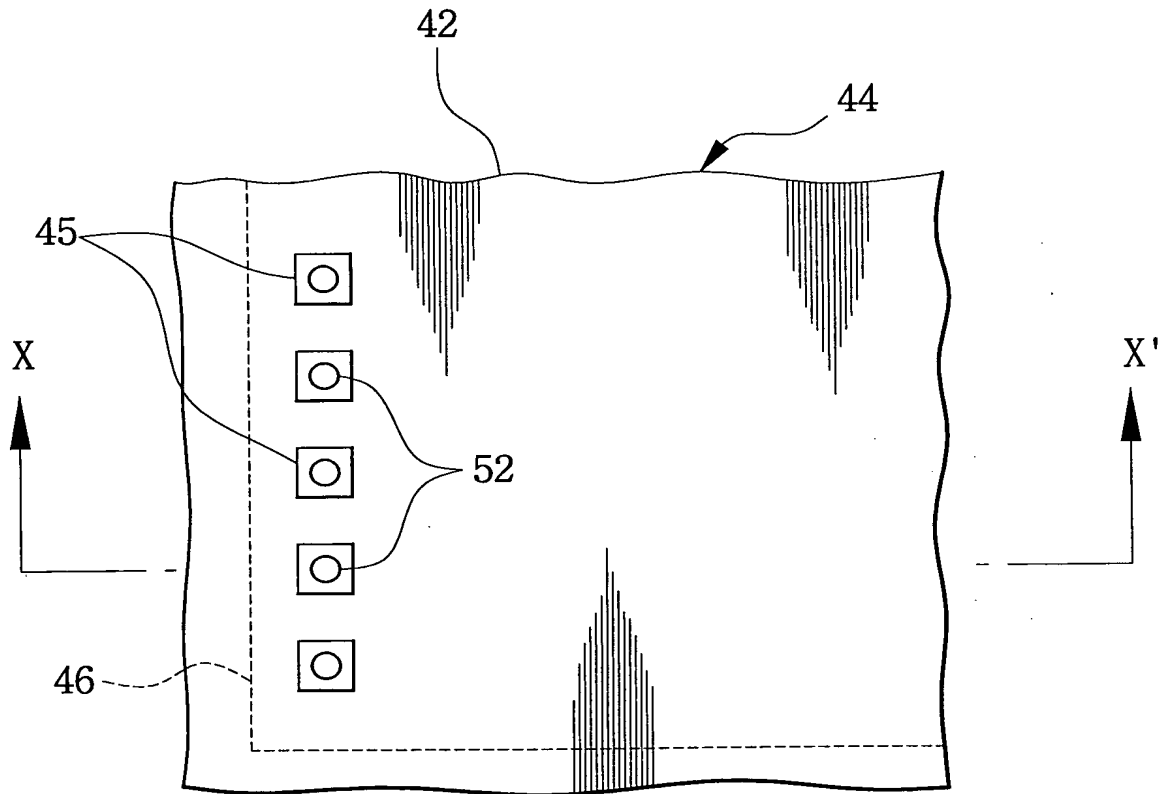
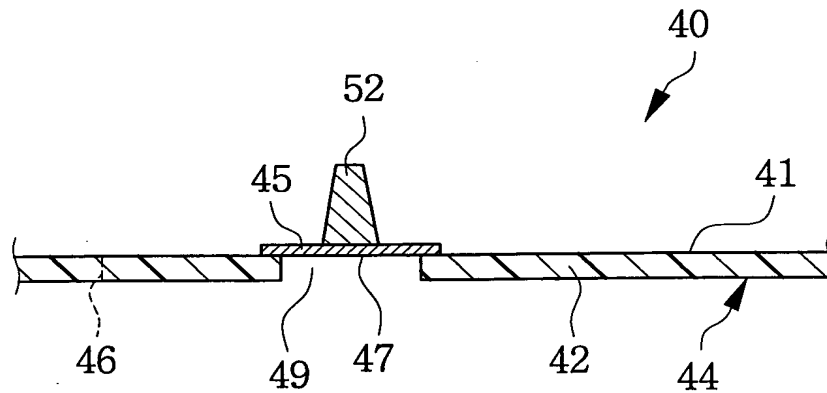
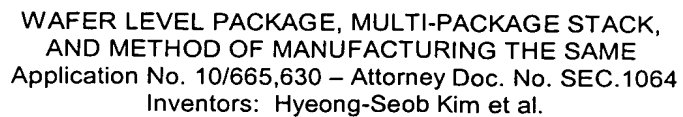


FIG .10





A cross-sectional view of a semiconductor device 30. The device features a substrate 39 with a trench 37' formed in its surface. A gate structure 31 is positioned within the trench 37'. The gate structure 31 includes a gate dielectric layer 33 and a gate electrode layer 35. A source/drain region 36 is located on the left side of the trench 37', and a source/drain region 32 is located on the right side. A gate spacer 38a is formed on the top surface of the substrate 39, adjacent to the trench 37'. A dashed line indicates a cross-section through the source/drain region 36. An arrow 34 points to the substrate 39, and an arrow 30 points to the overall device structure.

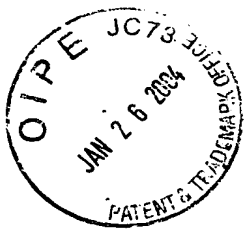


FIG .12b

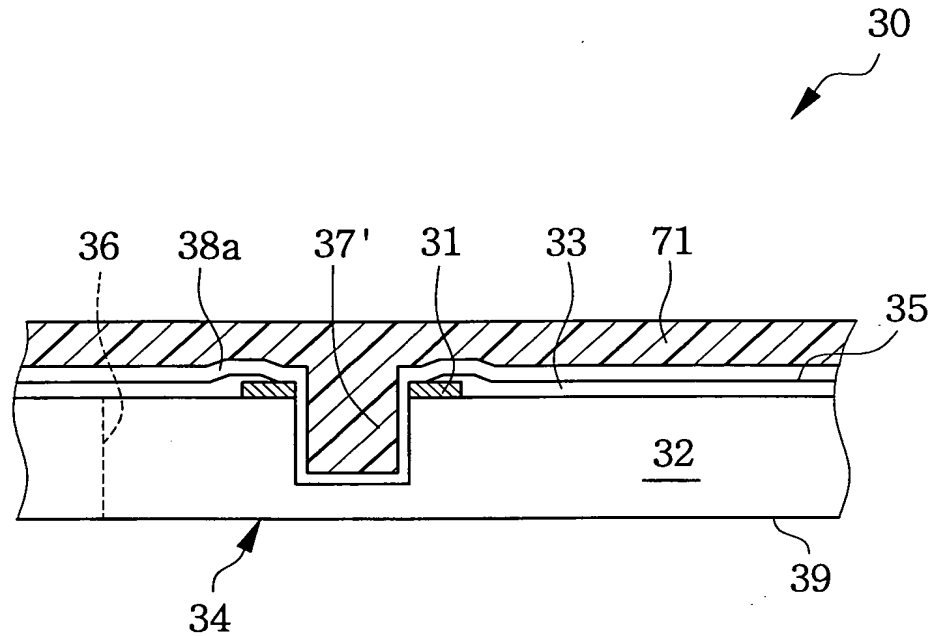
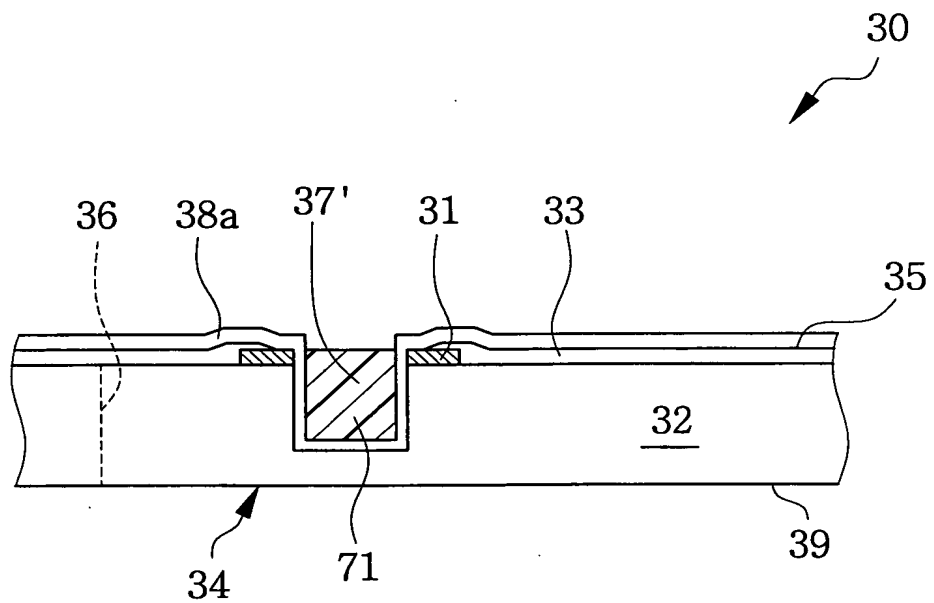


FIG .12c



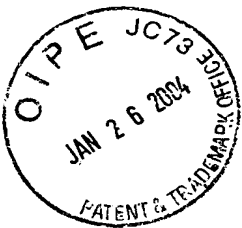


FIG .12d

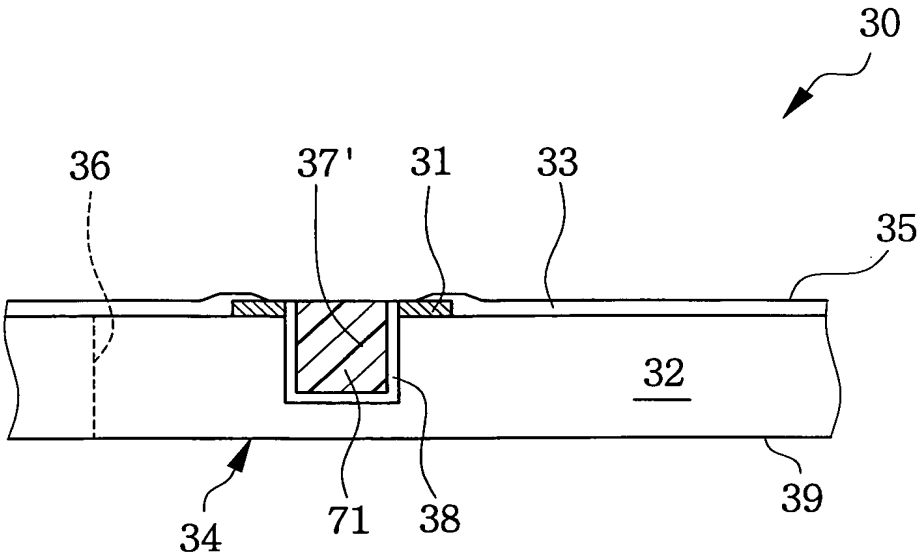
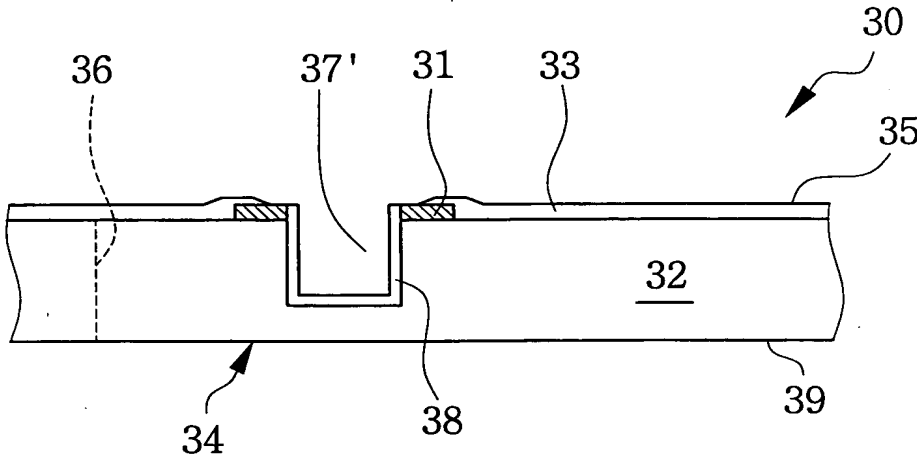
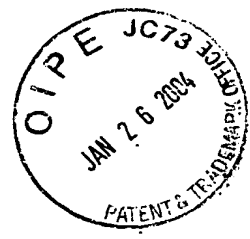


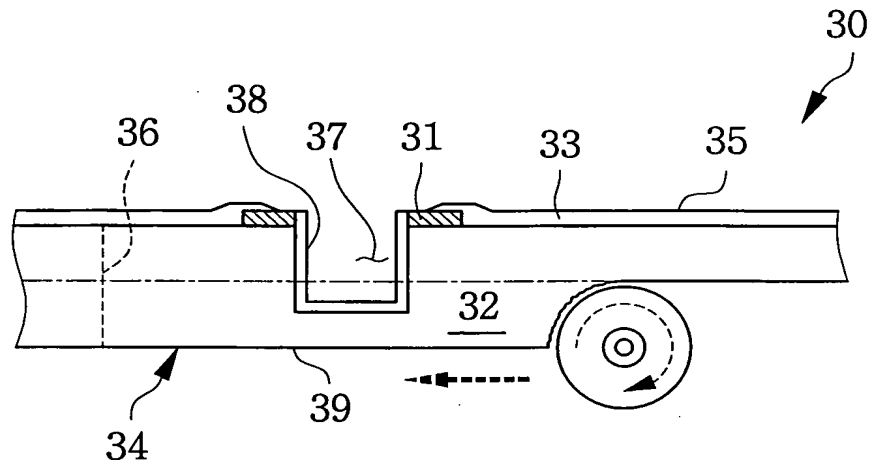
FIG .12e





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FIG .13



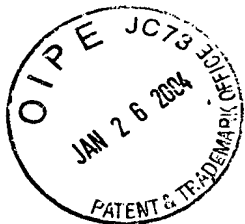


FIG .14

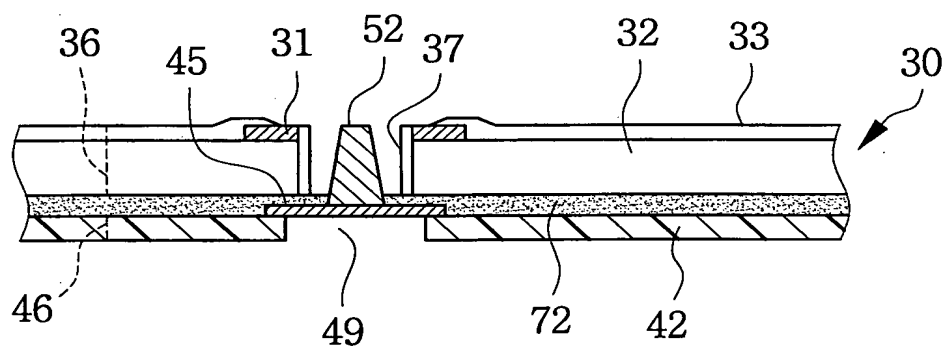
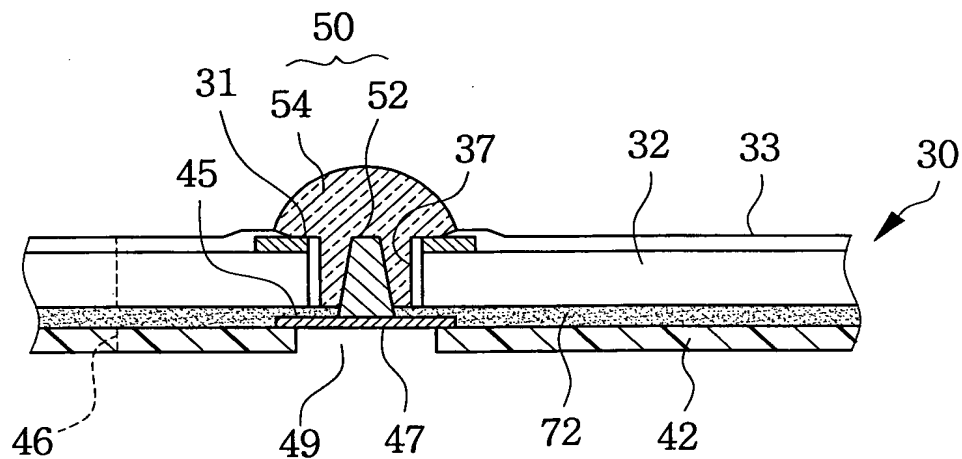
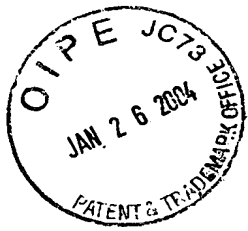


FIG .15





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FIG .18

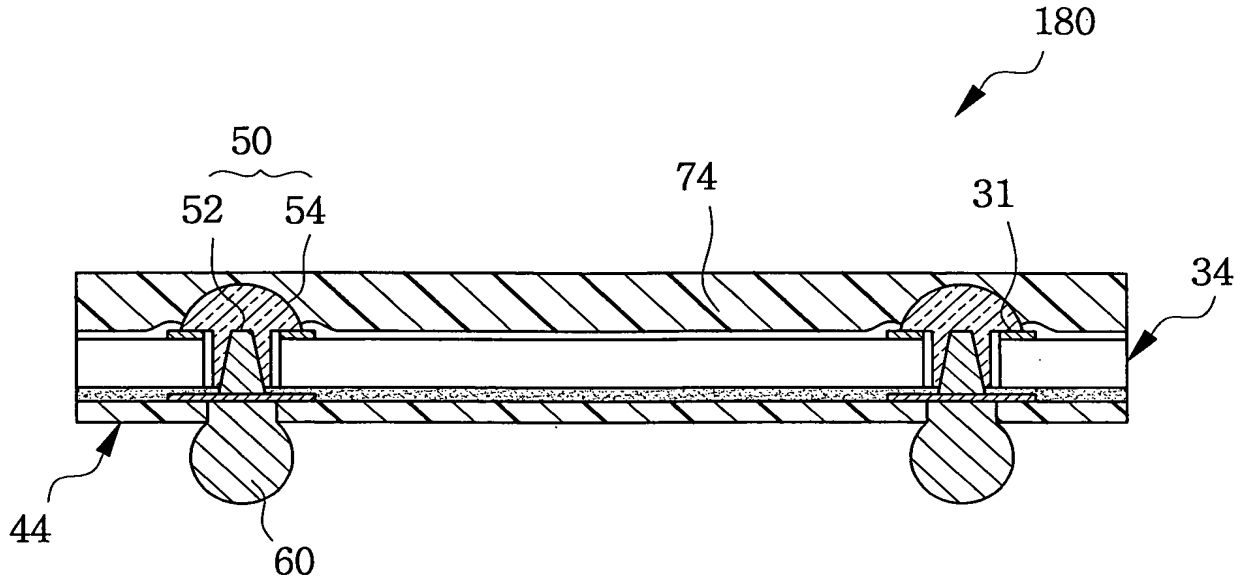
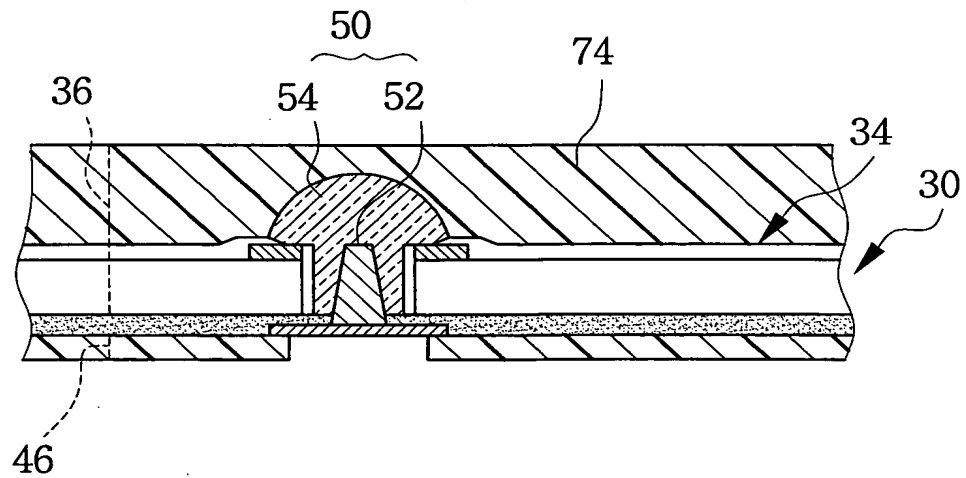
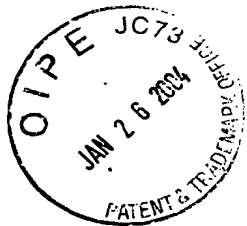


FIG .19





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FIG .20

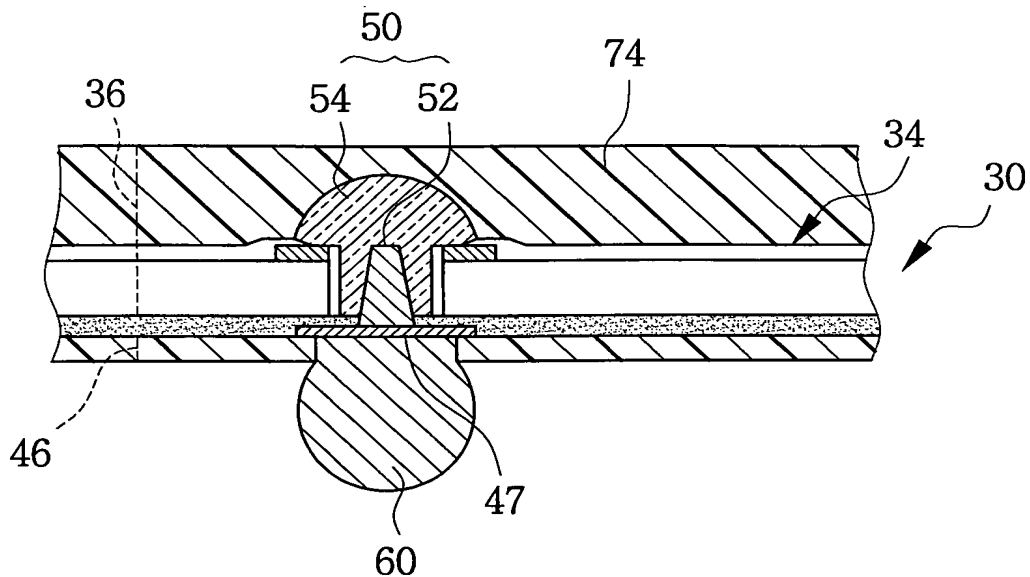
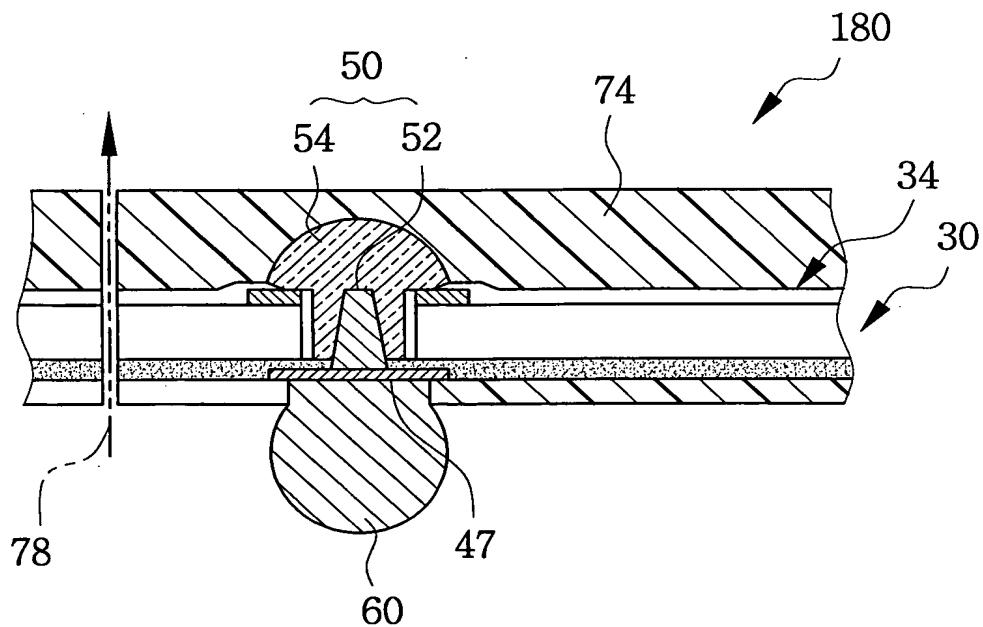


FIG .21



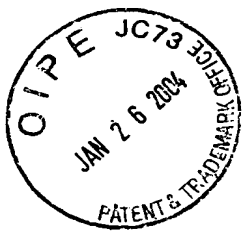


FIG .22

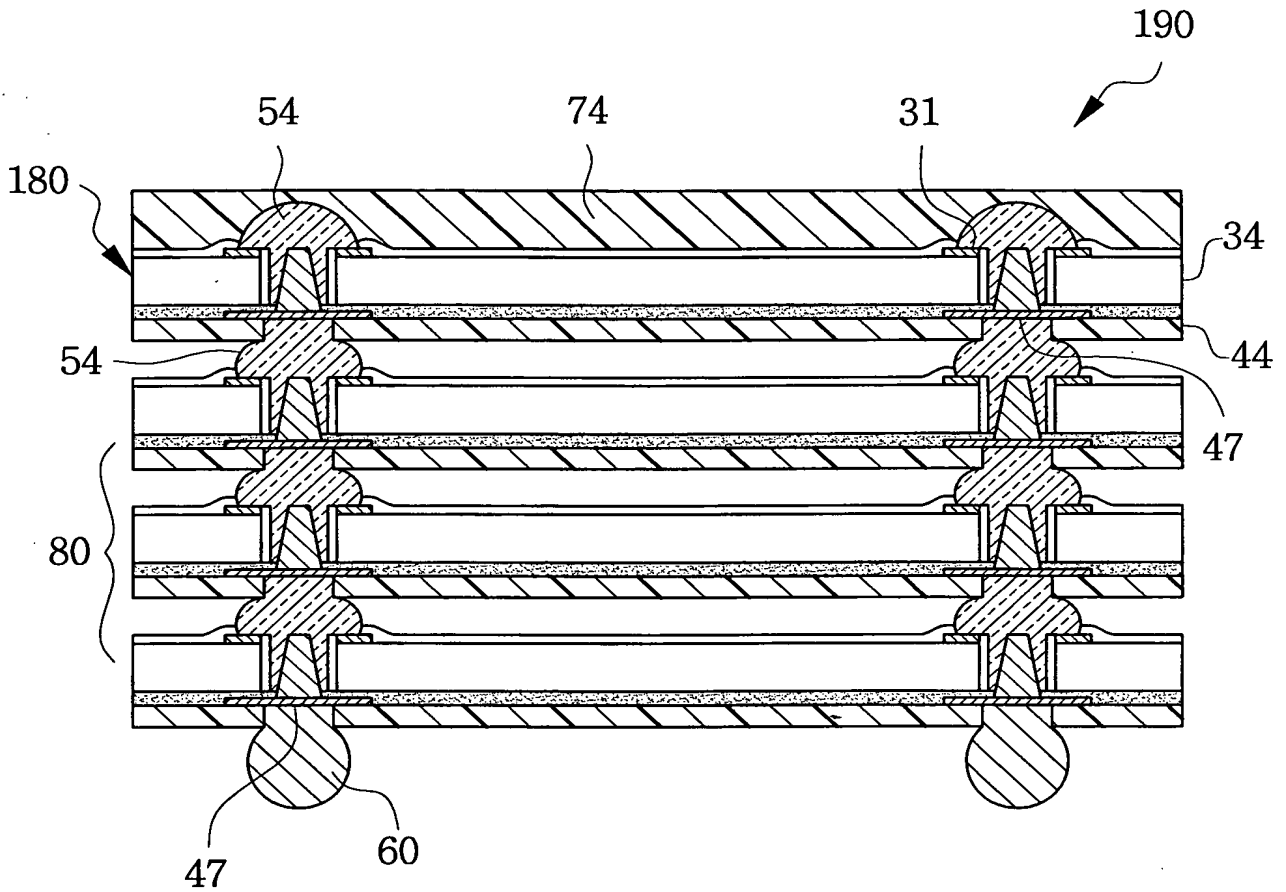
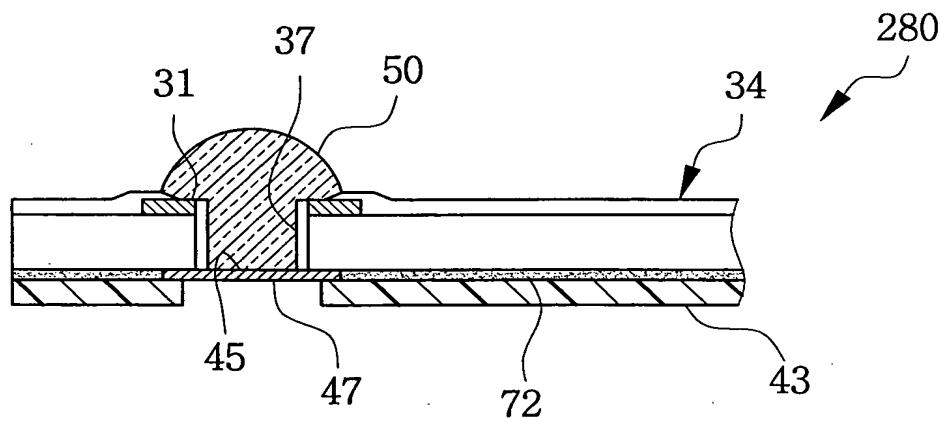


FIG .23



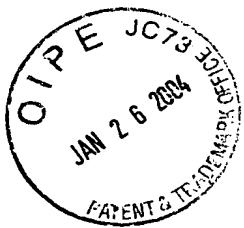


FIG .24

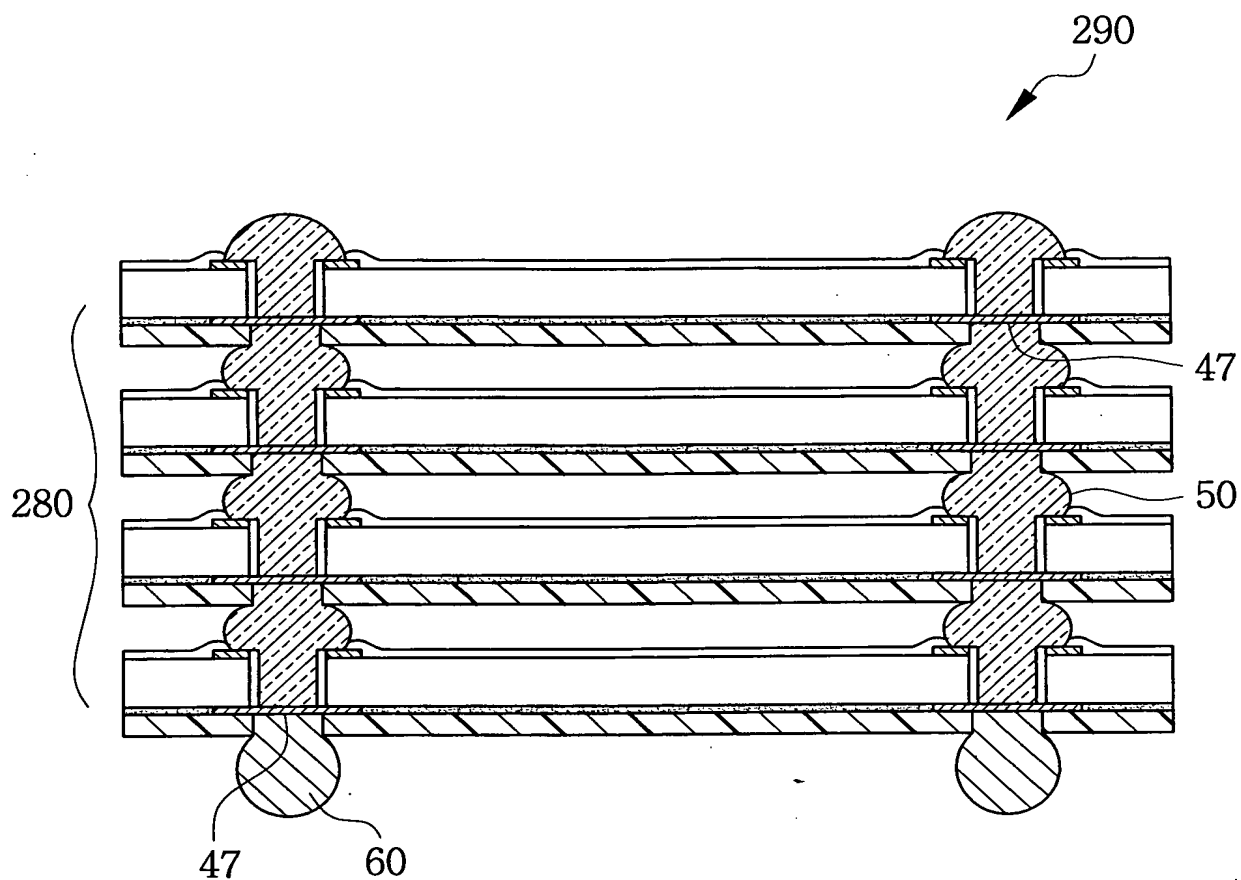
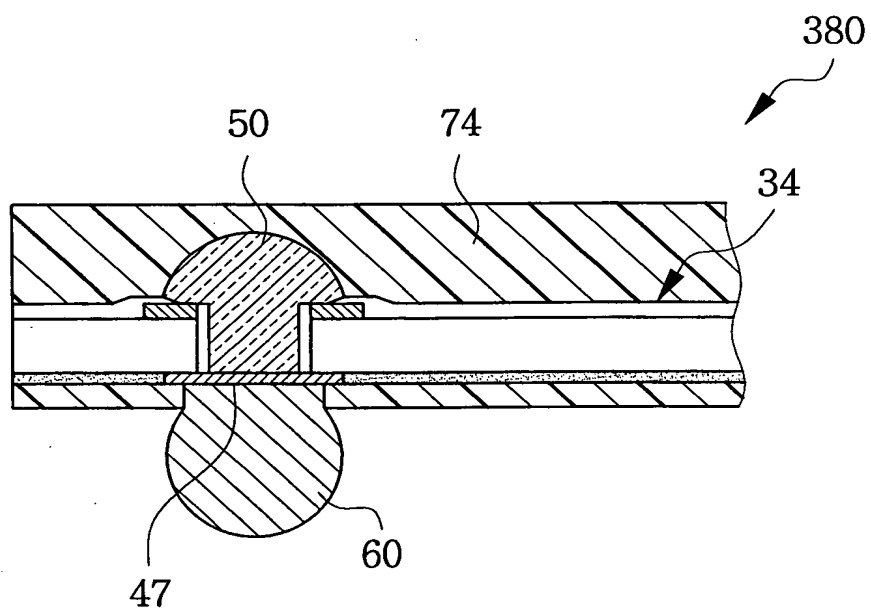


FIG .25



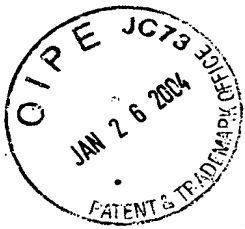


FIG .26

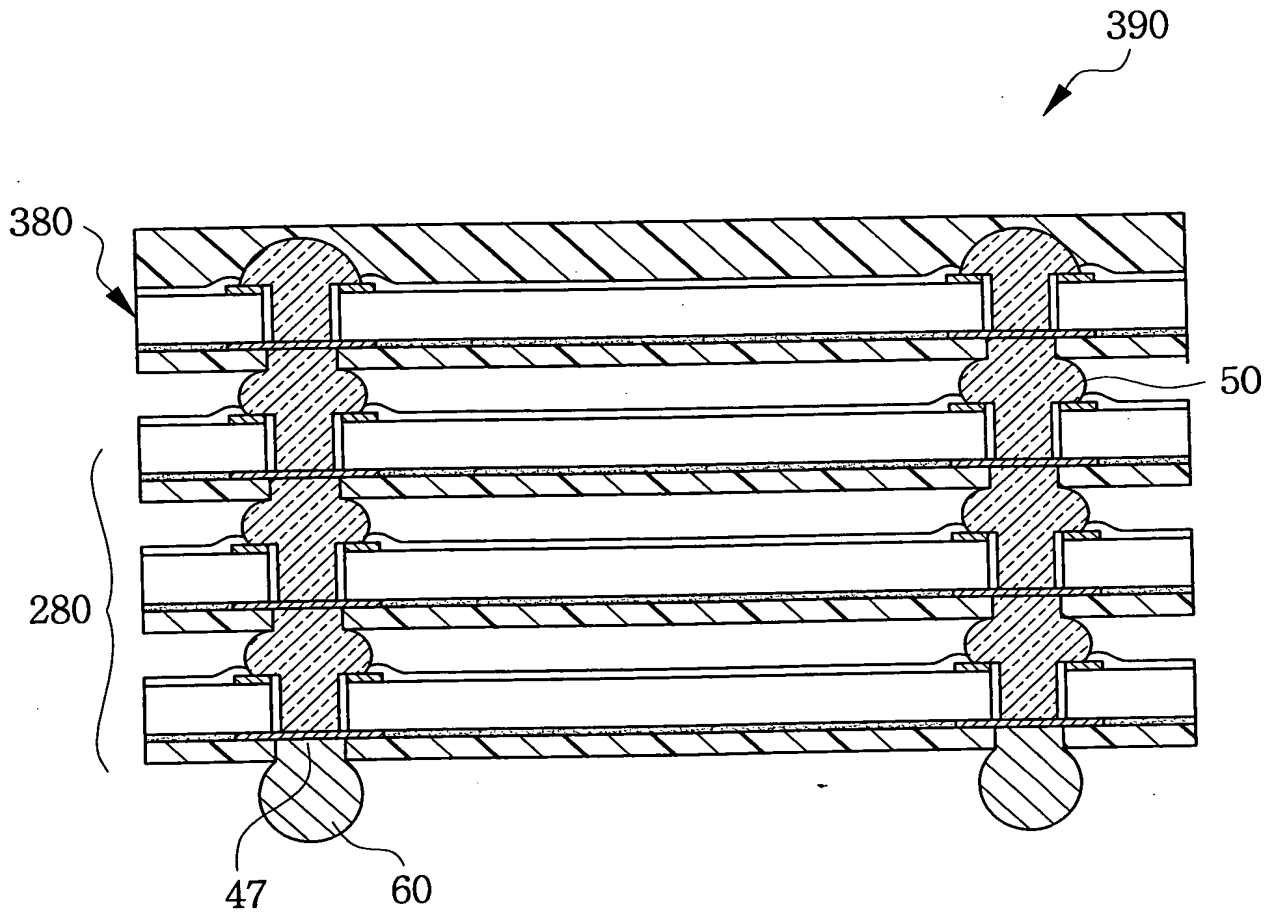
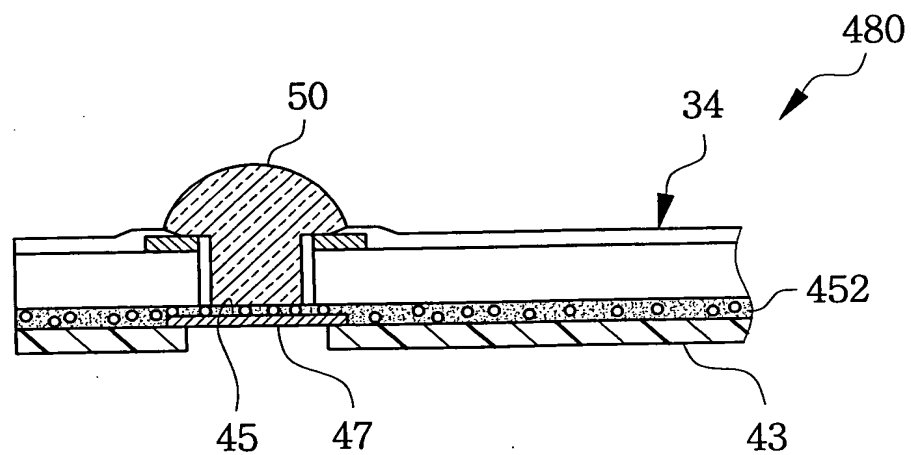


FIG .27



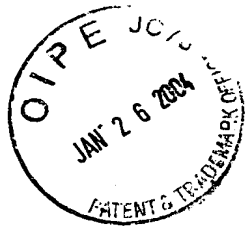


FIG .28

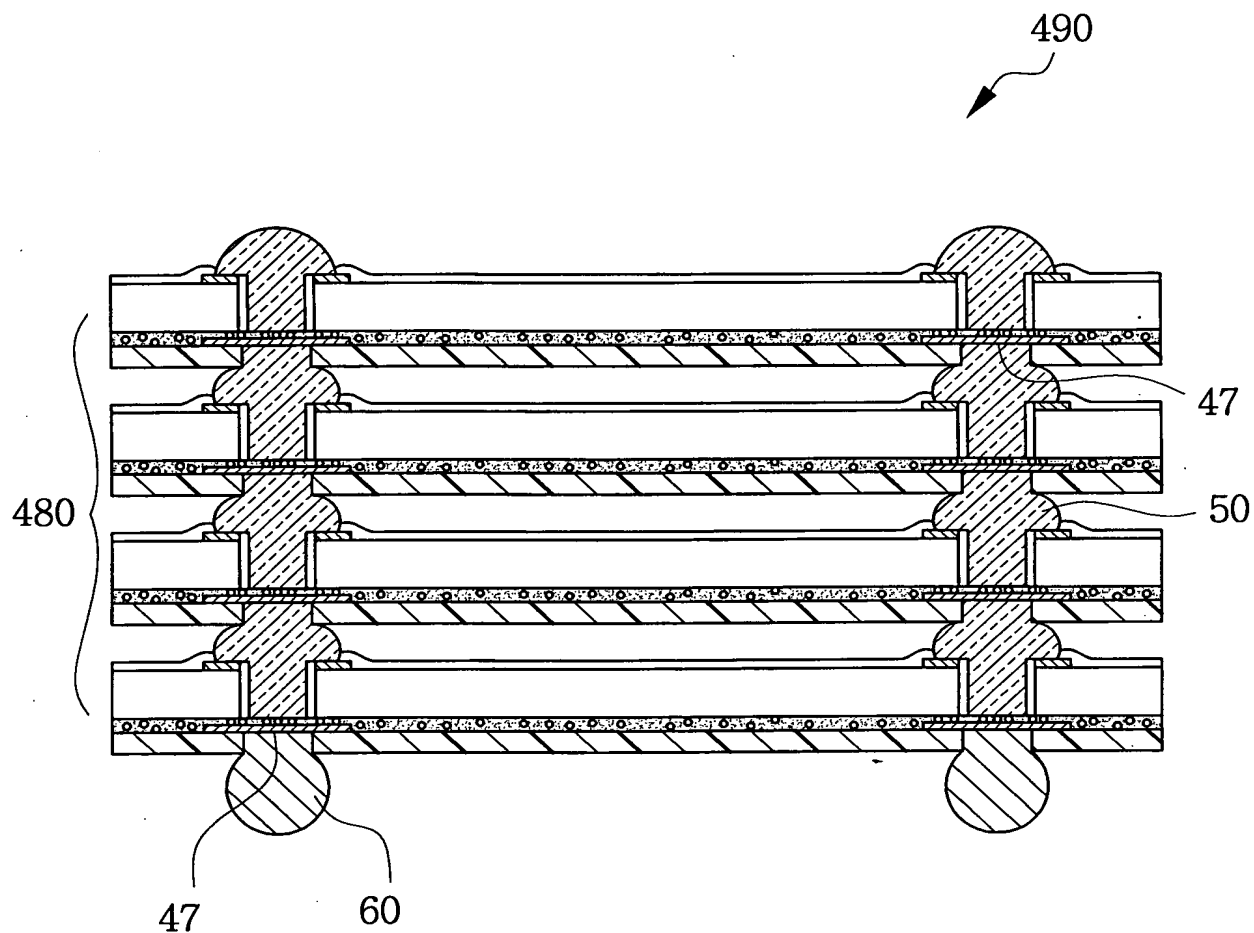
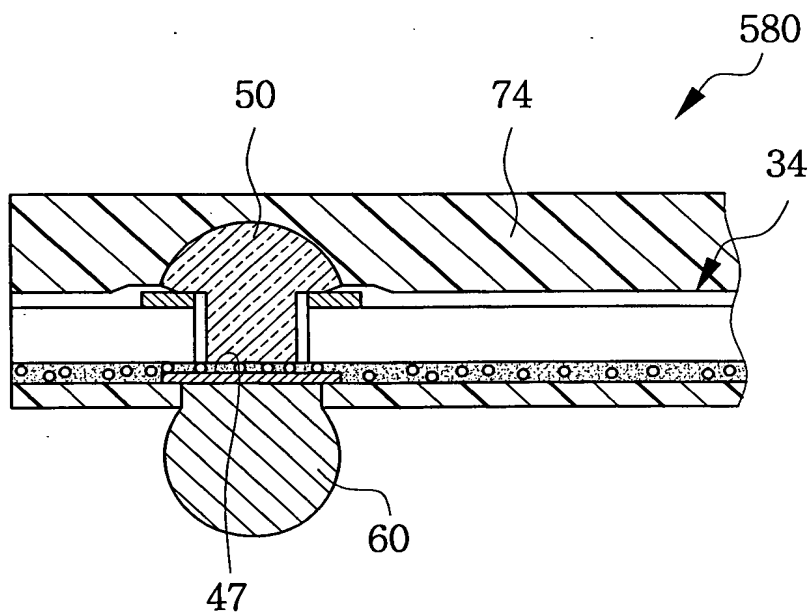


FIG .29



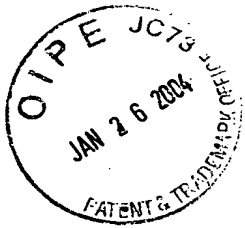


FIG .30

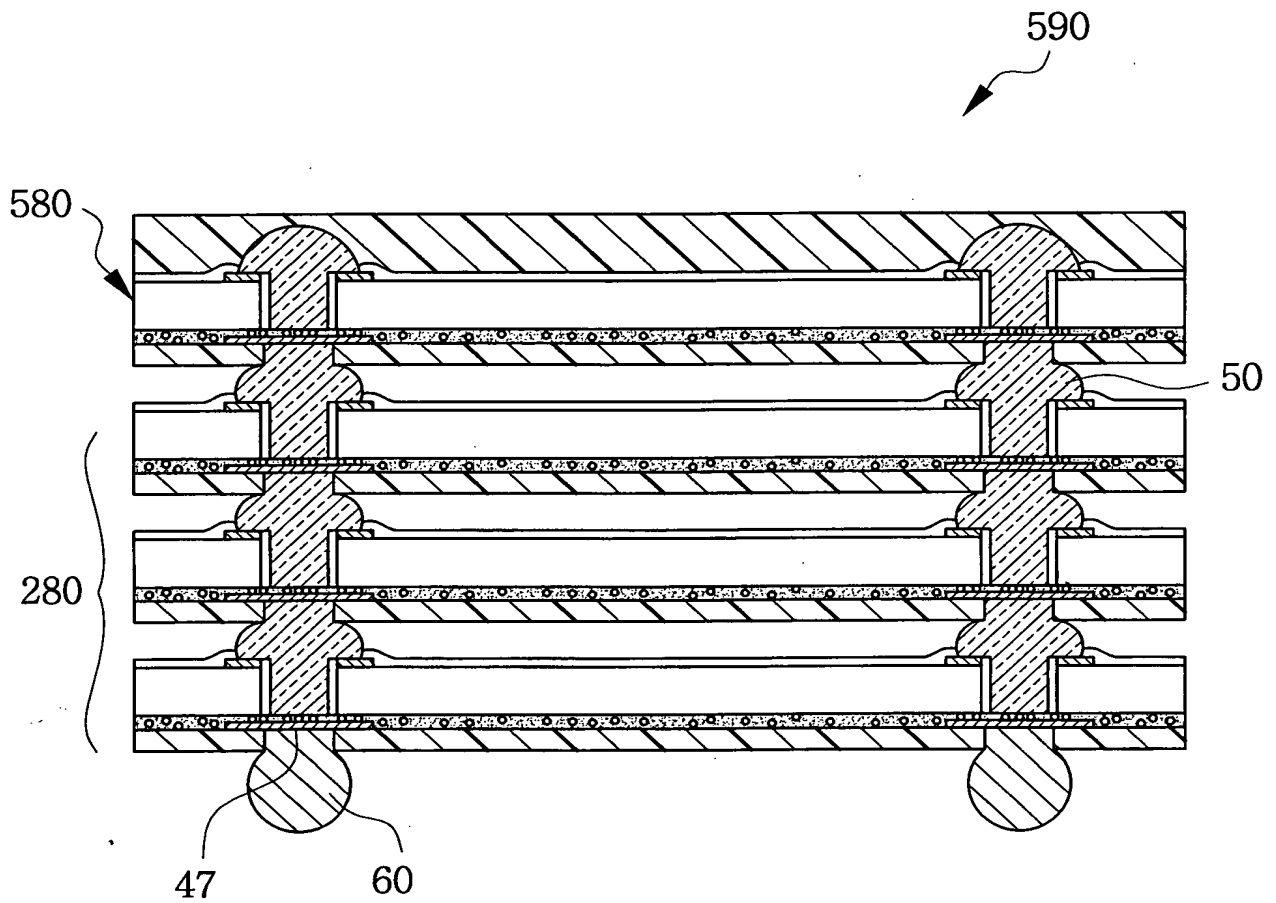




FIG .31

